MEMORY BUS TERMINATION WITH MEMORY UNIT HAVING TERMINATION CONTROL

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for a memory system using line termination circuits in each memory unit (e.g., integrated circuit memory device) are disclosed. The memory unit contains termination control logic that sets the state of a controllable termination circuit to control reflections on the data bus. The termination control logic determines the proper state for the termination circuit from the state of its memory unit, and in some cases, from the approximate state of the data bus as gleaned from commands decoded from the command/address bus. A termination configuration register on the unit can be used to define the appropriate termination state for each unit state and/or data bus state.